

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 2-4 and in the specification as originally filed, for example, on page 3, lines 12-16, on page 7, line 17 through page 8, line 2, on page 13, line 6. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 2, 6-13 and 16-20 under 35 U.S.C. §103(a) as being unpatentable over Mote, Jr. (U.S. Patent No. 5,630,110; hereinafter Mote) in view of Pole, II et al. (U.S. Patent No. 6,311,281; hereinafter Pole) and the background section of the specification (hereinafter Background) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 3 and 4 under 35 U.S.C. §103(a) as being unpatentable over Mote, Pole, and Background in further view of Tanoi (U.S. Patent No. 5,751,665) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 5 under 35 U.S.C. §103(a) as being unpatentable over Mote, Pole, and Background in further view of

Ogilvie et al. (U.S. Patent No. 6,038,629; hereinafter Ogilvie) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 14 and 21 under 35 U.S.C. §103 (a) as being unpatentable over Mote, Pole, and Background in further view of Finch et al. (U.S. Patent No. 5,513,319; hereinafter Finch) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 15 under 35 U.S.C. §103(a) as being unpatentable over Mote, Pole, Background and further in view of the I²C Bus specification has been obviated by appropriate amendment and should be withdrawn.

Mote, Pole, Tanoi, Ogilvie, Finch and the I²C Bus specification, alone or in combination, do not appear to teach or suggest the combination of (i) a first circuit configured to change a frequency of one or more clock signals in response to one or more first control signals, (ii) a second circuit configured to generate the one or more first control signals and a second control signal and (iii) a third circuit configured to generate a first reset signal in response to either the second control signal or a predetermined time period expiring, as presently recited in claim 1. Claims 18 and 19 include similar limitations. Therefore, Mote, Pole, Tanoi, Ogilvie, Finch and the I²C Bus specification, alone or in combination, do not teach or suggest each and every element of the presently pending claims 1, 18 and 19. As such, the presently claimed invention is fully patentable over the cited references and

the rejections should be withdrawn.

Claims 2-17 and 20-21 depend, either directly or indirectly, from either claim 1 or claim 19 which are believed to be allowable.. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

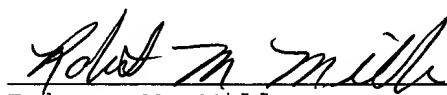
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

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